In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Previously presented) A method for placing a device in a selected mode of operation, the method comprising the steps of:

(a) initializing a device select signal into a first logic state;

(b) asserting the device select signal in a second logic state; and

(c) returning the device select signal to the first logic state within a first user-controlled time window which selects, at least in part, a mode of operation of the device.

2. (Original) The method in accordance with claim 1, where the step (a) of initializing a device select signal further comprises the step of placing the device select signal into an inactive logic state.

3. (Original) The method in accordance with claim 2, wherein the inactive logic state comprises a HIGH logic state.

4. (Original) The method in accordance with claim 1, wherein the step (b) of asserting the device select signal further comprises the step of placing the device select signal into an active logic state.

5. (Original) The method in accordance with claim 4, wherein the active logic state comprises a LOW logic state.

6. (Original) The method in accordance with claim 1, wherein the device includes a clock signal input and the step (c) of returning the device select signal to the first logic state within a first user-controlled time window further comprises the step of returning the device select signal

to the first logic state after the occurrence of a first transition of the clock signal, but before the occurrence of a second subsequent transition of the clock signal.

7. (Original) The method in accordance with claim 6, wherein the first transition of the clock signal comprises the second falling edge of the clock signal that occurs after assertion of the device select signal in a second logic state.

8. (Original) The method in accordance with claim 6, wherein the selected mode of operation is a reduced power consumption mode of operation, and the second subsequent transition of the clock signal comprises the tenth falling edge of the clock signal that occurs after assertion of the device select signal in a second logic state.

9. (Original) The method in accordance with claim 6, wherein the device is restored to normal operating mode by the additional steps of:

(d) asserting the device select signal in the second logic state; and

(e) returning the device select signal to the first logic state within a second user-controlled time window.

10. (Original) The method in accordance with claim 9, wherein the second user-controlled time window is defined by at least ten falling edges of the clock signal.

11. (Previously presented) A method for placing an integrated circuit device having a chip select (CS) input and a clock (CLK) input into a selected mode of operation, the method comprising the steps of:

(a) controlling the CS input of the device to place the CS input into an initial inactive logic state;

(b) placing the CS input into an active logic state to select the device; and

(c) within a first user-controlled time window defined by transitions of the CLK signal, returning the CS input to the initial inactive logic state selecting, at least in part, a mode of operation of the device.

12. (Original) The method in accordance with claim 11, wherein the initial inactive logic state is a HIGH logic state.

13. (Original) The method in accordance with claim 11, wherein the active logic state is a logic LOW state.

14. (Original) The method in accordance with claim 11, wherein the selected mode of operation is a reduced power consumption mode of operation, and the first user-controlled time window defined by transitions of the CLK signal comprises a time window beginning with the second falling edge of the CLK signal that occurs after CS is placed in an active logic state, and ending with the tenth subsequent falling edge of the CLK signal that occurs while CS is in the active logic state.

15. (Original) The method in accordance with claim 11, wherein the device is restored to normal operating mode by the additional steps of:

(d) placing the CS input into the active logic state to select the device; and

(e) within a second user-controlled time window defined by transitions of the CLK signal, returning the CS input to the initial inactive logic state.

16. (Original) The method in accordance with claim 15, wherein the second user-controlled time window is defined by at least ten falling edges of the CLK signal.

17. (Cancelled)

18. (Cancelled)

19. (Amended) A device comprising:

means for detecting logic state transitions at a device select input and a clock input;

means for changing operating mode of the device in response to a user-controlled number of logic state transitions at the clock input, occurring between logic state transitions at the device select input;

the means for detecting logic state transitions at a device select input and a clock input further comprising

clock divide logic and counter circuitry coupled to the serial clock signal and the device select signal, the clock divide logic and counter circuitry generating intermediate control signals including a first intermediate control signal that occurs after the second falling edge of the serial clock signal and a second intermediate control signal that occurs after the tenth falling edge of the serial clock signal; and

~~The device of claim 18,~~ wherein the means for changing operating mode of the device places the device in a first selected mode of operation in response to a first combination of logic state transitions, and places the device in a second selected mode of operation in response to a second combination of logic state transitions.

20. (Original) The device of claim 19, wherein the first combination of logic state transitions comprises between two and ten logic state transitions at the clock input, occurring between logic state transitions at the device select input.

21. (Original) The device of claim 19, wherein the second combination of logic state transitions comprises at least ten logic state transitions at the clock input, occurring between logic state transitions at the device select input.

22. (Original) An analog-to-digital converter comprising:

means for converting an analog input signal into a corresponding digital signal in response to a control signal;

means for outputting the corresponding digital signal in serial form in response to a serial clock signal;

means for generating at least one command signal in response to a number of serial clock signal cycles occurring between changing states of the control signal; and

means for selecting an operating mode of the analog-to-digital converter in response to the command signal.

23. (Previously presented) The analog-to-digital converter of claim 22, wherein the means for converting an analog input signal into a corresponding digital signal further comprises:

a track and hold circuit coupled to the analog input signal; and

a successive approximation analog to digital converter (ADC) coupled to the track and hold circuit.

24. (Original) The analog-to-digital converter of claim 22, wherein the means for outputting the corresponding digital signal further comprises:

a data multiplexer coupled to said means for converting the analog input signal and to said serial clock signal; and

a serial data output coupled to the data multiplexer.

25. (Original) The analog-to-digital converter of claim 22, wherein the means for generating at least one command signal further comprises:

clock divider and counter logic coupled to the serial clock signal and the control signal, wherein the clock divider and counter logic generates a plurality of command signals conditioned, at least in part, by the number of serial clock signal cycles occurring between changing states of the control signal.

26. (Original) The analog-to-digital converter of claim 25, wherein the means for selecting an operating mode of the analog-to-digital converter in response to the command signal further

comprises control and power management logic coupled to the control signal and the clock divider and counter logic.

27. (Original) An integrated circuit subsystem comprising:

a plurality of integrated circuit devices each having a signal input and a signal output, the devices interconnected such that a signal output of a preceding device is coupled to a signal input of a subsequent device, and the integrated circuit devices share common device select and serial clock input signals; and

control circuitry coupled to the device select and serial clock input signals, the control circuitry placing the plurality of integrated circuits into a DAISY CHAIN mode of operation in response to a user-controlled number of logic state transitions of the serial clock input signal occurring between logic state transitions of the device select signal.

28. (Original) An analog-to-digital converter having an analog input signal and a digital output signal corresponding to a digital representation of the analog input signal, the analog-to-digital converter comprising:

a conversion subsystem that converts the analog input signal into the digital output signal;

a range programming subsystem responsive to a device select input signal and a serial clock input signal;

such that full-scale input voltage range of the analog-to-digital converter is selected from among a plurality of full-scale input voltage ranges in response to a user-controlled number of logic state transitions of the serial clock input signal occurring between logic state transitions of the device select signal.